Задание 1. Выполнить кодирование состояний автомата, представленного на рисунке 3, в соответствии с индивидуальным вариантом из таблицы 1. Для этого заполнить таблицу 2.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Вариант | Набор | St0 | St1 | St2 | St3 |
| 5 | XC3S200 | 00 | 11 | 10 | 01 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | St0 | St1 | St2 | St3 |
| Q1Q0 | 00 | 11 | 10 | 01 |
| CNT | 0 | 1 | 1 | 0 |
| CNT\_EN | 0 | 1 | 0 | 1 |
| CNT\_CLR | 1 | 0 | 1 | 0 |

CNT = Q1

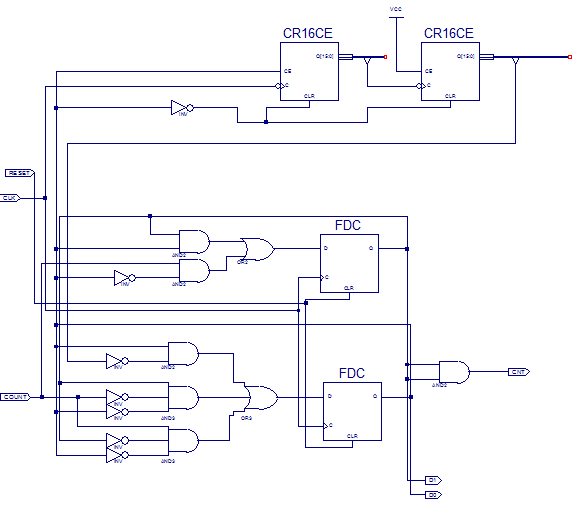
CNT\_EN = Q0

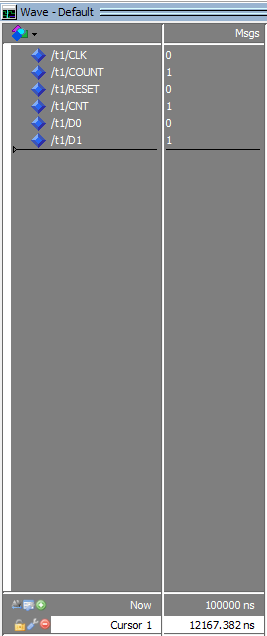
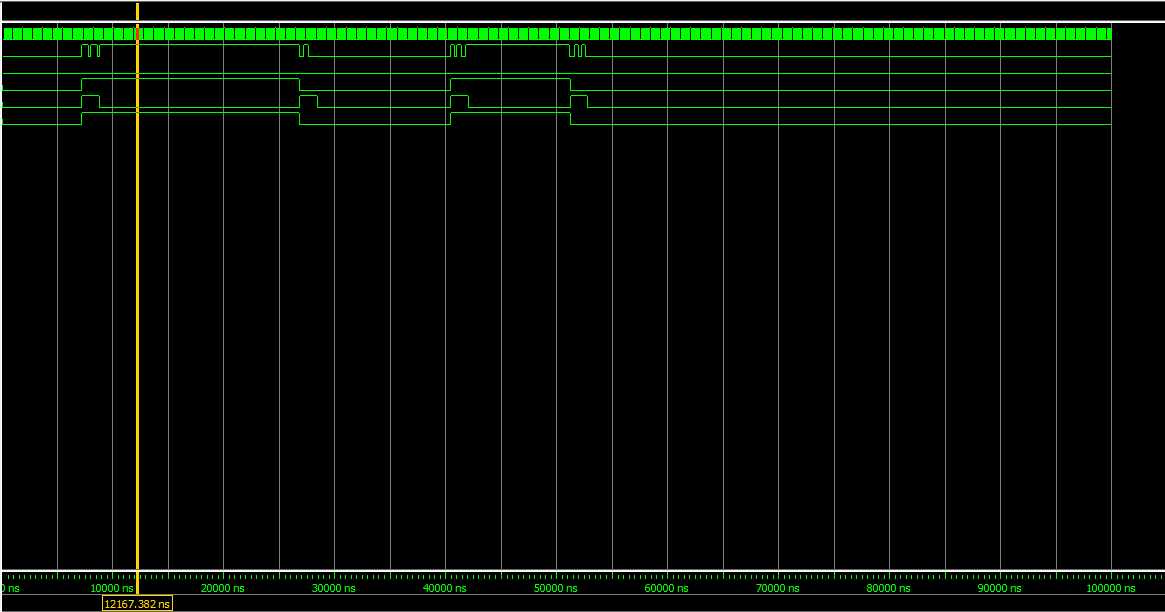
CNT\_CLR = /Q0;

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| count | Q[20] | Q1(t) | Q0(t) | D1 | D0 |
| 0 | X | 0 | 0 | 0 | 0 |
| 1 | X | 0 | 0 | 1 | 1 |
| X | 0 | 1 | 1 | 1 | 1 |
| X | 1 | 1 | 1 | 1 | 0 |
| 1 | X | 1 | 0 | 1 | 0 |
| 0 | X | 1 | 0 | 0 | 1 |
| x | 0 | 0 | 1 | 0 | 1 |
| x | 1 | 0 | 1 | 0 | 0 |

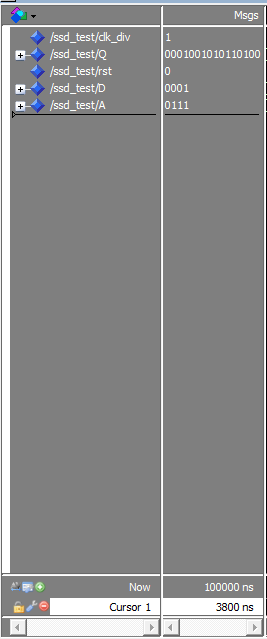
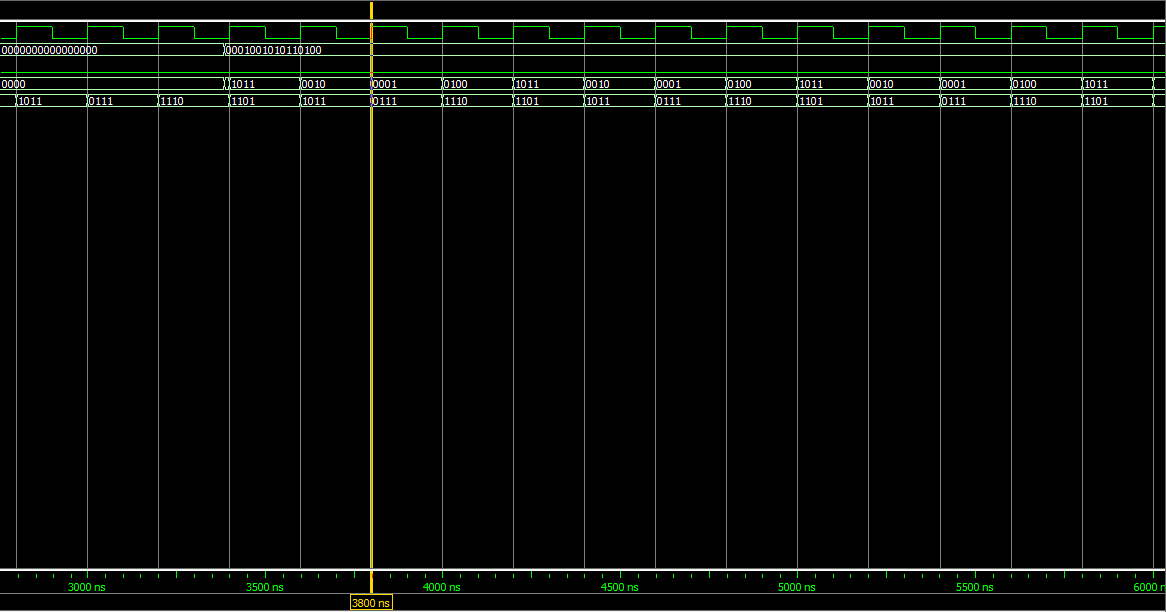
D1 = Q1Q0 v CNT /Q0

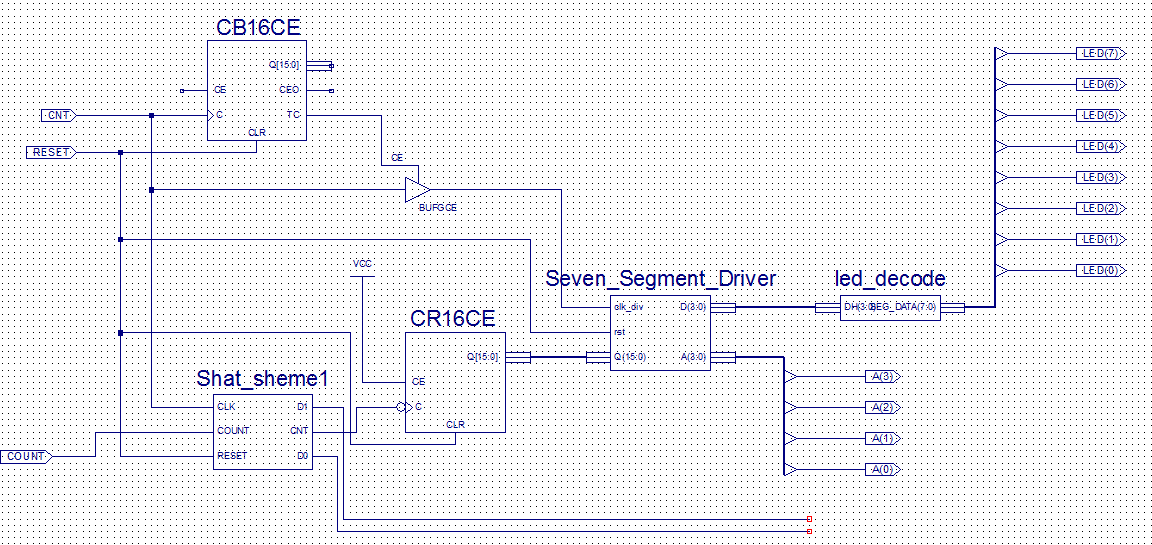
D0 = Q0 /Q20 v Q1 /Q0 /CNT v CNT /Q1 /Q0



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All values displayed in nanoseconds (ns)

Setup/Hold to clock CNT

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| Setup to | Hold to | | Clock |

Source | clk (edge) | clk (edge) |Internal Clock(s) | Phase |

------------+------------+------------+------------------+--------+

COUNT | 0.449(R)| 1.255(R)|CNT\_IBUFG | 0.000|

------------+------------+------------+------------------+--------+

Clock CNT to Pad

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| clk (edge) | | Clock |

Destination | to PAD |Internal Clock(s) | Phase |

------------+------------+------------------+--------+

A<0> | 8.882(R)|XLXN\_14 | 0.000|

A<1> | 8.553(R)|XLXN\_14 | 0.000|

A<2> | 8.704(R)|XLXN\_14 | 0.000|

A<3> | 8.799(R)|XLXN\_14 | 0.000|

D0 | 9.120(R)|CNT\_IBUFG | 0.000|

D1 | 8.817(R)|CNT\_IBUFG | 0.000|

LED<0> | 12.715(R)|XLXN\_14 | 0.000|

LED<1> | 12.944(R)|XLXN\_14 | 0.000|

LED<2> | 12.000(R)|XLXN\_14 | 0.000|

LED<3> | 12.173(R)|XLXN\_14 | 0.000|

LED<4> | 12.075(R)|XLXN\_14 | 0.000|

LED<5> | 13.085(R)|XLXN\_14 | 0.000|

LED<6> | 13.028(R)|XLXN\_14 | 0.000|

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Clock to Setup on destination clock CNT

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

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CNT | 1.836| | 1.844| 1.494|

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Analysis completed Sat Mar 30 17:57:05 2019

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.std\_logic\_arith.ALL;

entity LEDD is

PORT(

D: IN std\_logic\_vector(3 DOWNTO 0);

LED: OUT std\_logic\_vector (7 DOWNTO 0);

)

end entity LEDD;

architecture struct of LEDD is

begin

if D ='0000' then LED <= '0000001'

elsif D = '0001' then LED <= '1001111'

elsif D = '0010' then LED <= '0010010'

elsif D = '0011' then LED <= '0000110'

elsif D = '0100' then LED <= '1001100'

elsif D = '0101' then LED <= '0100100'

elsif D = '0110' then LED <= '0100000'

elsif D = '0111' then LED <= '0001111'

elsif D = '1000' then LED <= '0000000'

elsif D = '1001' then LED <= '0000100'

elsif D = '1010' then LED <= '0001000'

elsif D = '1011' then LED <= '1100000'

elsif D = '1100' then LED <= '0110001'

elsif D = '1101' then LED <= '1000010'

elsif D = '1110' then LED <= '0110000'

elsif D = '1111' then LED <= '0111000';

end architecture struct;